MEMORANDUM

TO: T, PWB America

FROM: Greg Lenihan

DATE: 4/2/2007

SUBJECT: Electrical Guidelines for PCB layout of the Data Acquisition System Module (DASM), Rev. 1.

PCB Number: 40972
Assembly Number: TBD

Attached are the Electrical, and in some cases, mechanical, guidelines for PCB layout of DASM. In addition to guidelines, a disk is also attached containing all required design media for layout. This includes OrCAD schematic, PADs netlist format, partslist (BOM), device data sheets, including associated PWB foot prints, as well as Microsoft Office drawings.

The designer should comply with the guidelines as best possible—especially critical signal routes and decoupling. Questions concerning layout should be directed to Greg Lenihan by landline at (949) 493-8181, Ext. 506, or by email at greg.lenihan@endevco.com and glenihan@n2.net.

1.0 Overview

The DASM is comprised of medium to high FPGA logic, memory, bus glue logic, isolated DC to DC converter, as well as a local bus mezzanine expansion interface.

The PWB form-factor is illustrated in Figure 1.1, which can be located on the design media disk. Along with these guidelines; the author will provide a layout scenario for clarification. The form-factor is part of a stack-thru topology, whereby the DASM can be the middle or top PWB of a 3 stack configuration; thus, complying with PWB dimension and form-factor is very critical. The entire stack assembly constitutes a Transducer Bus Interface Module (TBIM).

The designer should target an 8 to 10 layer PWB, utilizing 6 mil signal traces, except for controlled impedance routes, where this may not be possible, or for the obvious case of power and ground. One ounce copper as a minimum, with FR4 or Polymide type dielectric material, should be employed. The PWB must also implement a silk screen on layer one (component side) and on bottom layer.

The 8-layer stack up should be implemented in a manner such as:

Layer 1, Signal
Layer 2, Ground or Power plane
Layer 3, Signal
Layer 4, Ground and/ or Power planes
Layer 5, Signal
Layer 6, Signal
Layer 7, Ground or Power plane
Layer 8, Signal

Layer 1 (top side) and Layer 8 (bottom side) must be signal layers, which could also comprise non-plane power traces.

Layer 2 and Layer 7 must be planes, not signal or split-planes. This is for thermal reasons.

If an 8 layer board is not possible, then a 10 layer board will be acceptable with the following stack up:

Layer 1, Signal
Layer 2, Ground or Power plane
Layer 3, Signal
Layer 4, Ground and/ or Power planes
Layer 5, Signal
Layer 6, Signal
Layer 7, Ground or Power plane
Layer 8, Signal
Layer 9, Ground or Power plane
Layer 8, Signal

Layer 1 (top side) and Layer 8 (bottom side) must be signal layers, which could also comprise non-plane power traces.

Layer 2 and Layer 9 must be planes, not signal or split-planes. This is for thermal reasons.

1.1 PWB Form-factor

The PWB form-factor is illustrated in Figure 1.1.

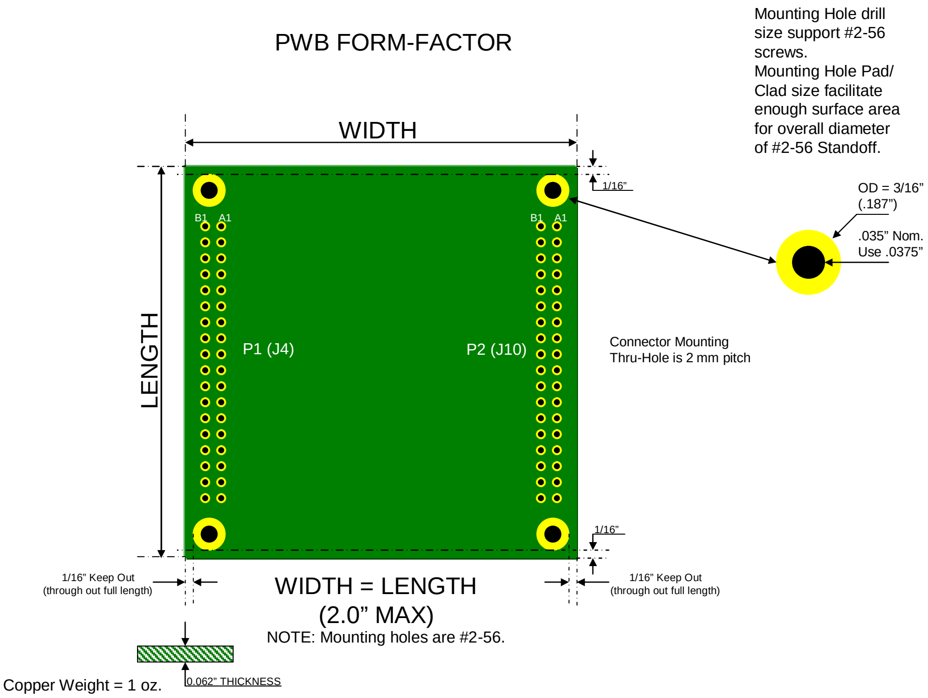


Figure 1.1: PWB Form-factor illustration.

From Figure 1.1, it can be seen that two, 2 X 18 position connectors are used for stack-thru. TEKA Interconnection Systems manufactures the stack-thru connector.

Figure 1.2 illustrates 3-stack topology, whereby DASM is either the middle or top board of the stack.

Figure 1.3 illustrates the I/O signal definition for stack-thru connectors. Notice, each connector contains an A and B row position.

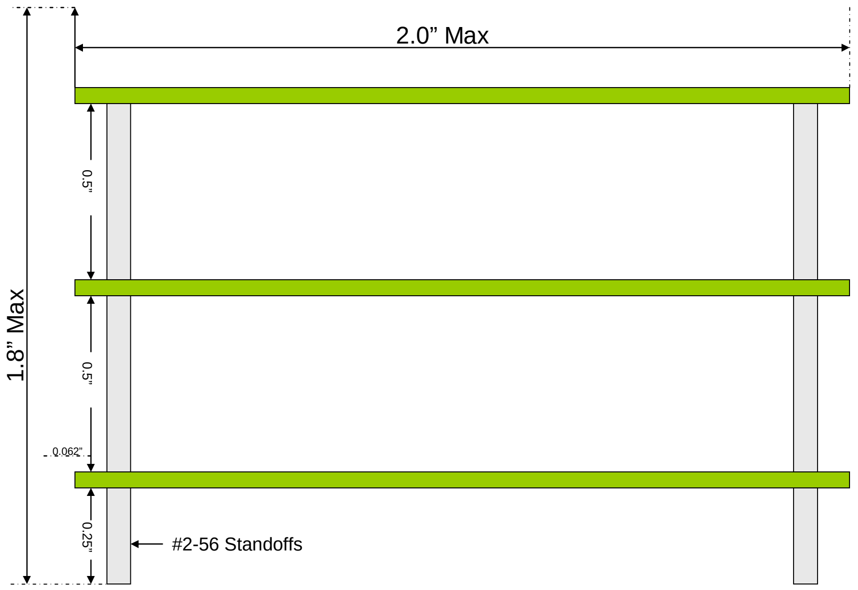


Figure 1.2: 3-stack illustration referred to as complete TBIM.

P1

PIN	ROW B	ROW A
1	GND	GND
2	AD0	CT0
3	AD1	CT1
4	AD2	CT2
5	AD3	3.3V
6	AD4	ALE
7	AD5	3.3V
8	AD6	TCLAIMn
9	AD7	GND
10	GND	SYSCLK
11	AD8	GND
12	AD9	IDPHRn
13	AD10	3.3V
14	AD11	TDPHRn
15	AD12	3.3V
16	AD13	SYSRESn
17	AD14	CERRn
18	AD15	GND

P2

PIN	ROW B	ROW A
1	GND	GND
2	BREQn	5V
3	BGNTn	5V
4	INTn	BDRESn
5	2.5V	2.5V
6	A17	A16
7	A19	A18
8	GND	A20
9	PGOOD	GND
10	2.5V	RXD
11	TXDEN	2.5V
12	MTOKA	TXD
13	NTOKI	5V
14	NTOKO	5V
15	NADD(1)	NADD(0)
16	NADD(3)	NADD(2)
17	ZV	ZV
18	ZV_RTN	ZV_RTN

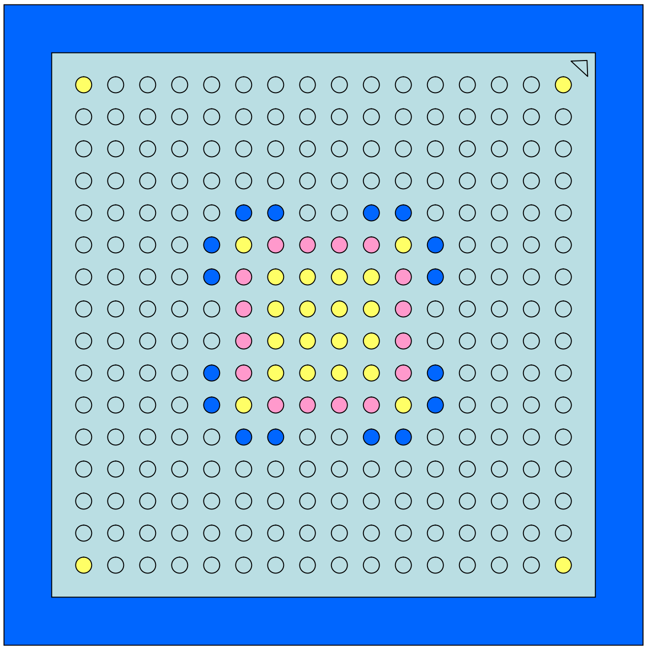
Figure 1.3: Signal I/O definition for stack-thru connectors.

2.0 Power , Grounds and Decoupling

The DASM comprises several power and grounds, including chassis ground. Table 2.0 summarizes power and ground definition with associated layout requirements.

Table 2.0: Power and Ground Definition and Requirements

Signal/ Power Name	Description	Trace Width	Notes
(+5V)	5 VDC Logic Power Input	40 Mils minimum or Split Plane	Associated In-Rush Caps, C11 and C12 should be kept in close proximity with DC-DC CONV., U6.
(+5VA)	5 VDC Analog Power	40 Mils minimum	C13 and C14 must be kept in close proximity with U6.
(VDDCR)	1.8 VDC Logic Power	40 Mils minimum	C18 must be kept in close proximity with U8.
(VDD)	2.5V FPGA Array Power	Split Plane. with GND split plane.	
(VDDP)	3.3 VDC Logic Power	Full Power plane required.	
(GND_SIGNAL)	Digital Ground	Full Power plane required.	
(GND)	Analog Ground	Split Plane. Could be split with VDD split plane.	
(ZV)	Zone Voltage (12-32 VDC)	24 mils minimum	
(GND_PWR)	Zone Voltage Return	24 mils minimum	
(LTV)	Level Translator Voltage (3.3 - 5 VDC)	24 mils minimum	
(VPP)	FPGA Programming Voltage +	12 Mils minimum	
(VPN)	FPGA Programming Voltage -	12 Mils minimum	
(GND_EARTH)	Chassis Ground	24 mils minimum	Chassis Ground should connect to 4 outer mounting holes



VDD Split plane must enclose FPGA 256-pin FBGA and its associated VDD decoupling.

Figure 2.0.1: VDD split plane illustration and description.

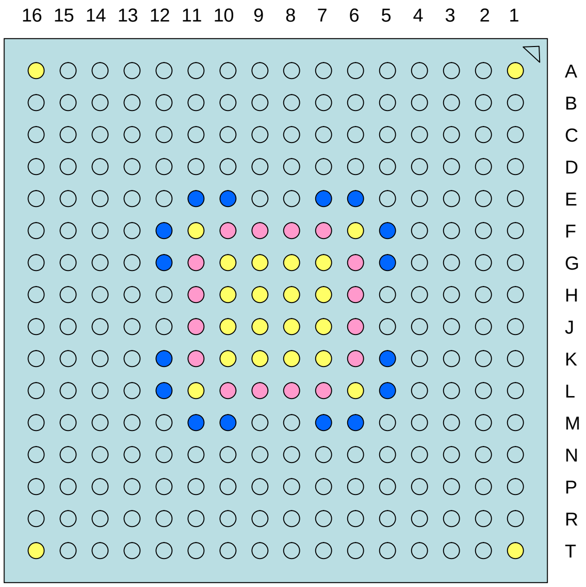
2.1 Decoupling

Decoupling capacitors should be kept close as possible to pertinent devices. For CMOS devices, decoupling should be kept to ground pins to minimize ground bounce (Ldi/dt). TTL and mixed signal circuits, such as reset and low signal analog circuits should be decoupled at power input: i.e., at VCC or VDD pin. Decoupling capacitors should be connected directly to associated power and ground planes.

2.1.1 FPGA Decoupling

The FPGA decoupling is extremely critical, and thus drawings are provided for clarity.

The APA600 is a Fine pitched Ball Grid Array.



LEGEND:
Yellow – GND_SIGNAL
Pink – VDD
Blue -- VDDP

Illustration of bottom side of APA600-FBGA 256-pin showing power and ground ball connections. Decoupling must be placed strategically, such that it is closest to respective power pin and shortest ground connection (to plane). This means that some decoupling can go on layer 1 up against FPGA; while the remaining decoupling will have to be placed on the last layer, such that it is within the FBGA interior close to respective power and ground planes.

Figure 2.1.1.1: APA600 FBGA decoupling scheme.

2.2 Chassis Ground Connections

Four EMI interconnections between Signal Ground and Earth Ground, via 1000 pF capacitors must be made. These capacitors, C50-C53 are located on sheet 4. Each capacitor must be placed at a PWB corner (one per corner).

3.0 Special Signal Routing

There are several special signal route types, including controlled impedance routing, signal routing for common mode, as well as the typical case of not routing control signals in parallel with bus signals, etc.

3.1 Clock and Clock Driver Circuitry

These signals are very critical.

Oscillator, U2, must be kept as close as possible to FPGA, U1. In addition, CLK133M must be kept short as possible. Isolation grounds (IGNDs) should enclose CLK133M.

3.2 Trace Buffer Bus Signals

Signal Name	Type	Description	Requirement
TBADD[19:0]	Bus	Address	Kept short as possible
TBDATA[15:0]	Bus	Data	Kept short as possible
TBWAITn	Control	Wait State Control	Kept short as possible
TBOEn	Control	Output Enable	Kept short as possible
TBWEn	Control	Write Enable	Kept short as possible
TBUBn	Control	Upper Byte Enable	Kept short as possible
TBLBn	Control	Lower Byte Enable	Kept short as possible
TBCEn	Control	Chip Enable	Kept short as possible
TBADVn	Control	Address Valid	Kept short as possible
TBCRE	Control	Clock Enable	Kept short as possible
TBCLK	Control	Clock	Kept short as possible

Bus signals should not be routed parallel with control signals. TBCLK should be isolated from all others and kept short as possible. If necessary, isolation grounds (IGNDs) should enclose TBCLK.

3.3 System Bus Signals

Signal Name	Type	Description	Requirement
AD[15:0]	Bus	Add./ Data Bus	55-65 ohm and kept close to J4.
CT[2:0]	Control	Cycle Type	55-65 ohm and kept close to J4.
ALE	Control	Address Latch En	55-65 ohm and kept close to J4.
TCLAIMn	Control	Transaction Claim	55-65 ohm and kept close to J4.

IDPHRn	Control	Initiator DP Ready	55-65 ohm and kept close to J4.
TDPHRn	Control	Target DP Ready	55-65 ohm and kept close to J4.
SYSRESn	Control	System Bus Reset	
CERRn	Control	CARD Error	
A[20:16]	Bus	Upper Address Bus	55-65 ohm and kept close to J10.
BINTn	Control	Bus Interrupt	Keep close to J10.
BREQn	Control	Bus Request	55-65 ohm and kept close to J10.
BGNTn	Control	Bus Grant	55-65 ohm and kept close to J10.

Bus signals should not be routed parallel with control signals.

3.4 Mezzanine Bus I/F Signals

Signal Name	Type	Description	Requirement
PIOA[7:0]	Bus I/O	Port A Data	Kept short as possible
PACTL[2:0]	Control I/O	Port A Control	Kept short as possible
PIOB[7:0]	Bus I/O	Port B Data	Kept short as possible
PBCTL[2:0]	Control I/O	Port B Control	Kept short as possible
PIOC[7:0]	Bus I/O	Port C Data	Kept short as possible
PCCTL[2:0]	Control I/O	Port C Control	Kept short as possible
PIOD[7:0]	Bus I/O	Port D Data	Kept short as possible
PDCTL[2:0]	Control I/O	Port D Control	Kept short as possible
PORTAEN	Control	Port A Enable	
PORTBEN	Control	Port B Enable	
PABLEV3	Control	Port A/B Level	

Bus signals should not be routed parallel with control signals.

3.5 Network Signals

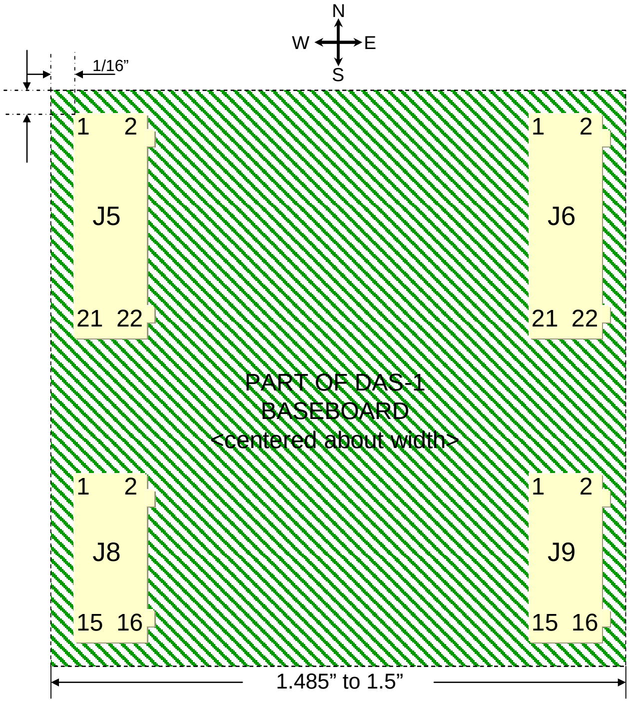
The following are network signals:

RXD
TXDEN
TXD
MTOKA
NTOKI
NTOKO
NADD[3:0]

RXD and TXD should be kept isolated from each other as well as other signals, including Local and System Bus signals.

4.0 Expansion Bus Mezzanine I/F

The connector mezzanine interface, comprised of J5, J6, J8, and J9, should be laid out in accordance with Figure 5.0. The drawing in Figure 4.0 illustrates how connectors should be pinned out, as well as position. It should be noted that all 4 connectors facilitate the mounting or installation of a DAS mezzanine PWB. Positioning of the mezzanine connector interface connectors should be such that J5/J8 and J6/J9 pairs are aligned vertically, and the entire combination pairs are centered about the board width. Positioning of the combination pairs must not obstruct the southern connector interfaces, nor extend beyond southern board edge, and further must not obstruct DC to DC converter, U6.



JST Receptacle Connector (22R-JED) Notches represent even pin number side. Connectors are inset 1/16” from board edges.

JST Receptacle Connector (16R-JED) Notches represent even pin number side. Connectors are inset 1/16” from board edges.

Figure 4.0: DASM mezzanine connector placement and pin reference.

5.0 Example or Pseudo Layout

In general, the 4 distinct bus interfaces discussed in Section 3.0 should be kept away from each other where possible.

At the onset, this example layout is more for clarity. However, there are some physical placement musts, in regards to board side. The following components ***must*** be located on side 1:

> All connectors
> DC to DC converter, U6

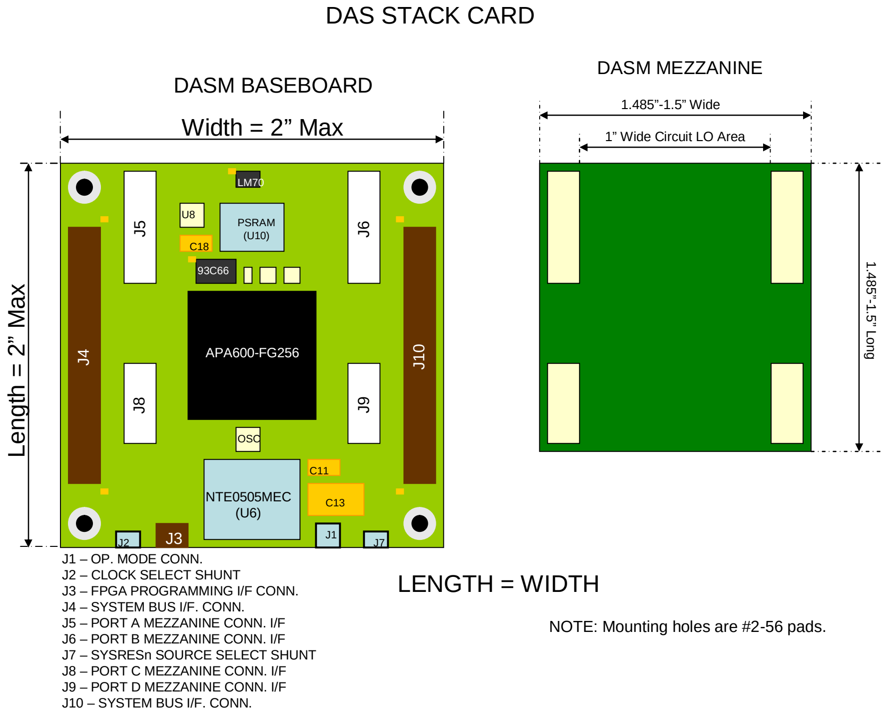


Figure 5.0: Example layout illustration, showing major components, including mezzanine board, only.